

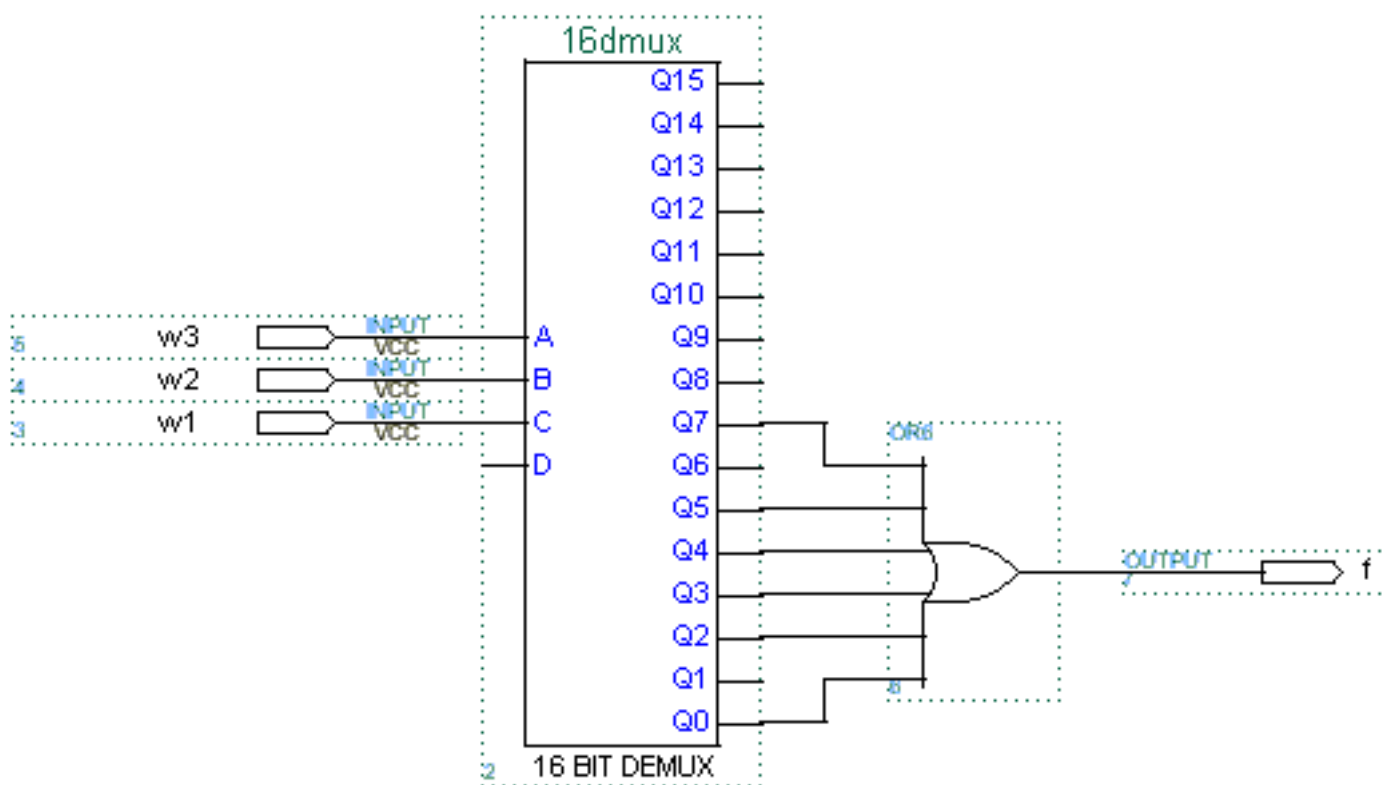
Laborbericht Labor 2

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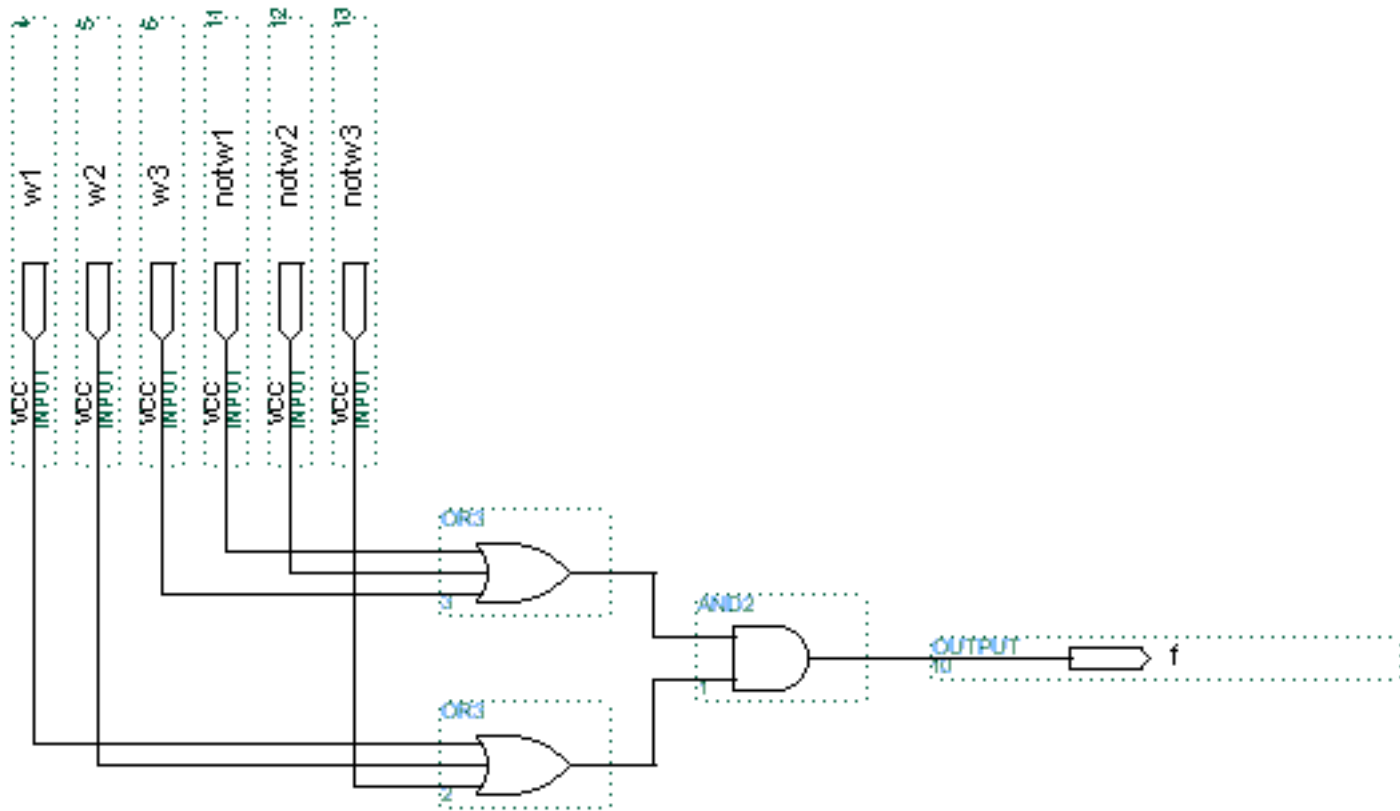
23. Dezember 2000

Aufgabe A

1.

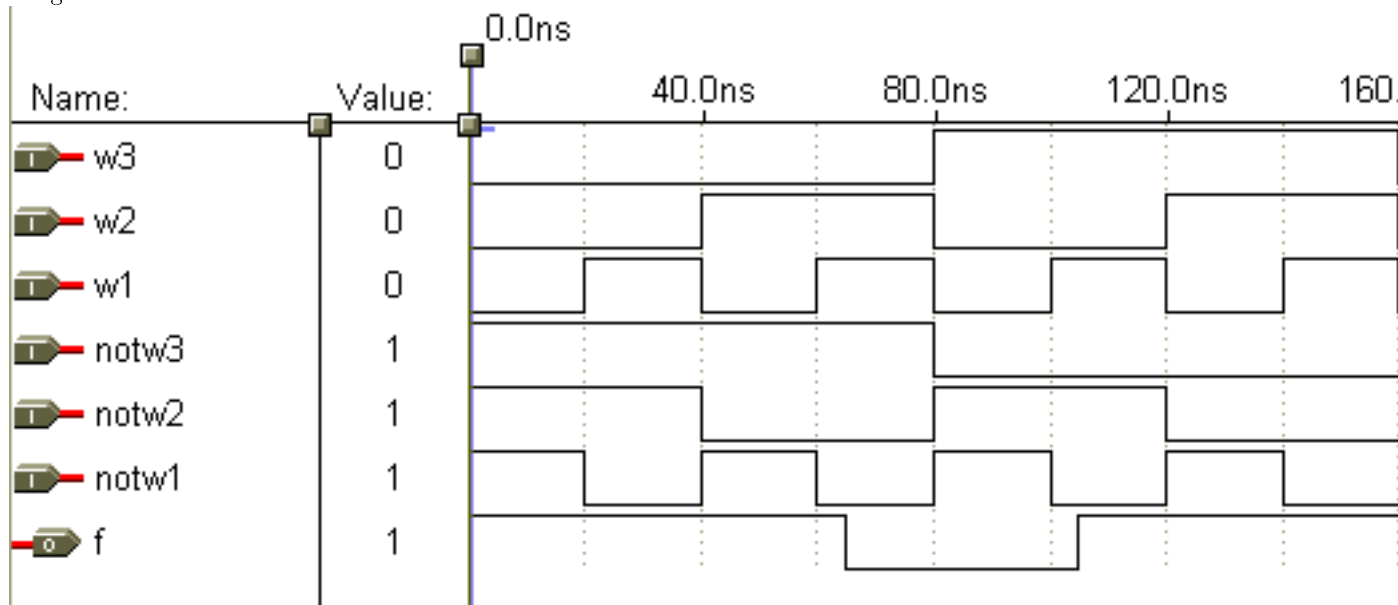


2.

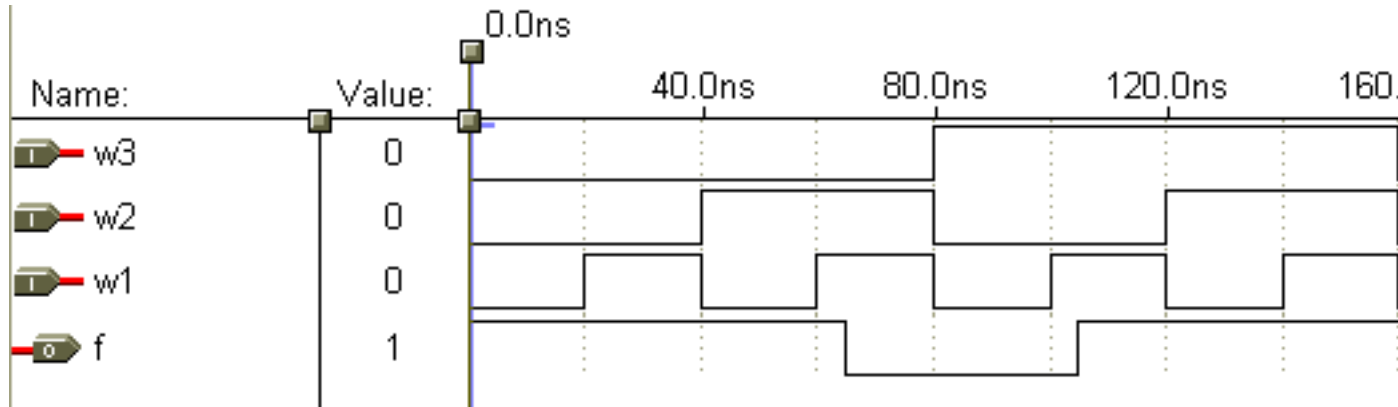


3.

Zeitdiagramm für AND-OR:



Zeitdiagramm für MUX:



4.

MUX:

```

LIBRARY ieee;
USE ieee.std_logic_1164.all;
ENTITY labor2_a4 IS
PORT(w1,w2,w3:IN STD_LOGIC;
f: OUT STD_LOGIC;
);
END labor2_a4;
ARCHITECTURE MUX OF labor2_a4 IS
BEGIN
g<=(NOT a1 AND NOT a3) OR (a2 AND a3) OR (a1 AND NOT a2) OR (NOT a1 AND
a2) OR (a1 AND a3);
END MUX;

```

AND/OR:

```

LIBRARY ieee;
USE ieee.std_logic_1164.all;
ENTITY labor2_a4_gatter IS
PORT(w1,w2,w3 : IN STD_LOGIC;
f: OUT STD_LOGIC);
END labor2_a4_gatter;
ARCHITECTURE Gatter OF labor2_a4_gatter IS
BEGIN
f<=(w1 OR w2 OR NOT w3) AND (NOT w1 OR NOT w2 OR w3);
END Gatter;

```

Aufgabe B

```

- VHDL '93
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_unsigned.all;
ENTITY labor2_b1 IS
PORT(
i: in std_ulogic_vector(0 to 7);    - input
o: out std_ulogic_vector(0 to 2);   - output
v: out std_ulogic);                - valid-bit
END labor2_b1;
ARCHITECTURE PRIOENC OF labor2_b1 IS
BEGIN

```

- Möglich waere serielle Realisierung, aber
- unpraktisch...

```

o <= "111" WHEN i(7)='1' else
      "110" WHEN i(6)='1' else
      "101" WHEN i(5)='1' else
      "100" WHEN i(4)='1' else
      "011" WHEN i(3)='1' else
      "010" WHEN i(2)='1' else
      "001" WHEN i(1)='1' else
      "000" WHEN i(0)='1' else "ZZZ";
WITH i SELECT
v <='0' WHEN "00000000",
  '1' WHEN OTHERS;
END PRIOENC;

```

2.

Simulation ist korrekt, leider nicht als Ausdruck möglich, da zuwenig Speicher. Ausdruck wird auf Wunsch nachgereicht.

Aufgabe C

1.

```

LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY labor2_c IS
    PORT(
        i: in std_logic_vector(0 to 3);    - input BCD
        o: out std_logic_vector(0 to 6));  - output 7Segment
END labor2_c;

ARCHITECTURE PRIOENC OF labor2_c IS
BEGIN
    with i select
        o <= "1110111" when "0000",      - 0      00000
            "0010010" when "0001",      - 1      1    2
            "1010101" when "0010",      - 2      1    2
            "1011011" when "0011",      - 3      33333
            "0111010" when "0100",      - 4      4    5
            "1101011" when "0101",      - 5      4    5
            "1101111" when "0110",      - 6      66666
            "1010010" when "0111",      - 7
            "1111111" when "1000",      - 8
            "1111011" when "1001",      - 9
        - Pseudotetraden
            "1111110" when "1010",      - A
            "0101111" when "1011",      - b
            "0001101" when "1100",      - c
            "0011111" when "1101",      - d
            "1101101" when "1110",      - E
            "1101100" when "1111",      - F
            "0000000" when others;
END PRIOENC;

```

2.

sh. Aufgabe B 2

Bemerkung

Andreas testet VHDL-Simulator SAVANT. Wenn Simulator läuft, können die Testvektoren der VHDL-Programme auf Wunsch nachgereicht werden. Probleme gab es beim Snapshot der Zeitdiagramme.